[Hardware Enforced Virtual Sequentiality]

Abstract of DisDisclosure

A mechanism processes memory reads and writes in a packet processor. Each memory access has an associated sequence number and information is maintained allowing the detection of ordering conflicts. The mechanism is placed between a processing element and a memory system such that write data is buffered and both reads and writes are recorded. When an ordering conflict is detected, based on a strict or alternate ordering model, a restart signal is generated and the entries for the associated sequence number are flushed. When the work associated with a sequence number has completed, a signal is made so that associated write data can be sent to the memory system and the entries for that sequence number can be flushed.

Figures